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AN ASSESSMENT OF TRENDS IN INTERCONNECTION TECHNOLOGIES AND THEIR IMPLICATIONS FOR FUTURE ORIENTED ARAB ELECTRONICS INDUSTRIES

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Introduction

In a most fundamental sense, the two basis elements for achieving electronic product hardware functionality are electronic / electrical devices and wiring . Before the integrated circuit era set in, electronic/electrical devices consisted strictly of individual discrete components, i.e. transistors, diodes, resistors, capacitors, etc. Electronic product hardware functionality was realized by interconnecting (wiring) these devices according to the wiring network dictated by the circuit /system design . The interconnection /wiring media consisted of individual wires, wire harnesses, connectors, cables and what was then the "new" technology of printed circuit boards (PCBs) . The interconnection terminations, where required, were generally either solder, or solderless (wire-wrapped, connector fit,...). Indeed the PCB may well be viewed as the first step in realizing integrated "components" in the electronics industry in the form of "integrated wires" .

Subsequently of course, beginning in the early 60s , the far more revolutionary concept of integration proved to be the semiconductor integrated circuit (SIC) . The profound impact of SICs as the central driving force behind the electronics industry and its rapid growth and pervasiveness has been felt for several decades . Current and projected developments in IC material and process developments clearly indicate a sustained profound impact for at least another two decades .

While this paper is not about integrated circuits per se, it is necessary to emphasize for the purpose of the paper's theme, that integrated circuit technology provided simultaneously for the integration of "discrete" electronic /electrical components as well as their associated interconnections .

The progress of integration and complexity associated with successive generations of integrated circuits is usually expressed in terms of the transistor device density and minimum device feature achieved . What is rarely explicitly highlighted is the concomitant achievement of higher density/finer feature IC interconnection capability . Indeed from the total system interconnection perspective, IC chips provided the most efficient and cost-effective "wiring" medium . These attributes derive directly from IC material and process technologies associated with generating in-situ intrachip "microconnections" and "microwires" as part of the overall IC wafer fabrication process .

The above interconnection dimension of the IC proper will be further illuminated in the course of this paper . In fact it will be a particularly useful reference point against which to gauge the current and projected progress and developments in interconnection technologies . These will constitute the main subject matter for

this paper and they will be discussed and evaluated within a unified perspective based on a three-tiered interconnection hierarchy relating to the IC package , the hybrid circuit and the printed circuit (Fig.1). The next levels of interconnection namely those of backplanes, cables and connectors, though important will not be addressed in this paper .

A comprehensive and unified approach to the interconnection aspects of electronic products is increasingly becoming mandatory if electronic products are to be developed, designed and manufactured cost-effectively and competitively in an increasingly global electronics world market environment . This will necessitate an important reorientation in the manner in which electronic products are developed and designed, whereby the interconnection design is viewed as an integrated and fundamental part of the entire development and design process, and not as a less glamorous and less significant aspect of it . Such a premise also sets the stage for an important orientation of R and D activities to encompass interconnection technologies alongside, and on a par with, other R and D activities relating to the development, design and manufacture of electronic devices, circuits and systems .

1 . Factors underlying the need for a growing emphasis on off-chip interconnection technologies

Developments in integrated circuits have had a profound and simultaneous impact on electronic products and systems on several fundamental levels . These include :

* Higher degrees of system integration leading to increased system functionality and reduced size and weight .

* Improved system performance , i.e. higher speed and lower power consumption .

* Lower system costs .

* Higher system reliability .

It is significant to note however that while such system/equipment attributes have been largely imparted by developments in ICs, developments in interconnection technologies over the last two decades have also had a positive impact in relation to all the factors above, though to a much lesser degree . This can be traced to the following considerations :

a) IC technology consistently stole the limelight by demonstrating an incessant and overwhelmingly greater capability in significantly enhancing electronic system cost effectiveness .
Such an environment drew very heavy R & D investments towards

integrated circuit R & D , thus limiting more significant investments that could have been channeled to interconnection technologies . In particular, research in academic institutions in interconnection technologies was totally lacking .

b) In addition to the impact of the above "bandwagon" IC effect, a further disincentive was created as a result of the overall attitude generally prevailing towards interconnection technologies which were (unjustifiably) considered "low-tech" and relatively unglamorous relative to the exciting ongoing and anticipated action in ICs.

c) In the small and medium scale integration (SSI and MSI) IC generations the intermediate pace of evolutionary developments in (off-chip) interconnection technologies seemed relatively adequate . These developments largely related to printed circuit and hybrid circuit technologies . It is particularly to be noted that the state of the art of IC performance capability at the time was not compromised as a result of embedding ICs into the interconnection circuit /system network . This was because the performance capability (i.e. bandwidth) of the "transmission channel" represented by this interconnection network was significantly superior to the IC performance capability . This network thus represented an essentially transparent transmission medium . Overall system speed was therefore largely limited by inherent IC device speed .

The above considerations combined clearly did not create an imperative or environment for hastening the pace of interconnection technology development . This does not however imply that such developments were not significant . The impact of such developments may be seen in Fig.2 which reflects trends in interconnection densities measured against the backdrop of IC density trends [1] .

With the advent of LSI and particularly, VLSI, many of the considerations above have changed significantly , and new elements have also further set in . These are broadly addressed in what follows and shall be elaborated in following sections .

a) The increasing levels of integration on a single chip coupled with the increasingly higher inherent speed of integrated circuits have generated, particularly for logic chips, new constraints on chip packages and chip-to-package interconnections . As a result traditional chip packaging represented by the venerable dual-in-line package (DIP) is increasingly being viewed as inadequate both from a performance (speed) as well as a physical (size) point of view .

b) Size and performance factors related to the second level interconnection (PCB) were also found to be inadequate for the VLSI age, as were those associated with the intermediate (hybrid circuit) interconnection level .

c) The increasingly competitive global electronic market is forcing electronics equipment manufacturers to adopt a more comprehensive approach to cost-effective equipment development and design whereby cumulative incremental advantages can make the difference between success and failure . Such an approach in fact underlies the resounding success of Japanese products in the world market .

Interconnection technologies in recent years have thus clearly come under significant pressure both from the device end due to the advent and growth of VLSI, as well as from the equipment end . Current and future trends in interconnection technologies intended to relieve this interconnection bottleneck are discussed in the following sections . Their significance and anticipated impact are also highlighted . The thrust of these efforts is to smoothen the physical and performance transition between the microworld of integrated circuit chips and the macroworld of electronic circuits, subassemblies and products . A more fundamental and unified approach to "macrointegration" is warranted if the full benefits of current and future developments in "microintegration" are to be attained . Such a realization has spurred many new initiatives inrecent years some of which have involved the support of related research programs at academic institutes [2].

2 . Chip Packaging and Surface Mount Assembly Trends

2.1 Developments in chip packaging

The dual-in-line package (DIP) has been the chip packaging workhorse for over two decades . However with the rising input /output (I/O) requirements (pin count) of high density /complexity VLSI logic chips , the DIP has become grossly inadequate . The lead fanout pattern associated with such a package style inherently compromises the performance (speed) and density advantages of high pin count VLSI chips .

In recent years alternate package styles have evolved to circumvent this problem , many of which are being incorporated at a rapid rate by semiconductor device manufacturers in their device product lines . These new package styles are indicated in Fig. 3 . The two major distinctive features of most of these package styles (PLCC,LCC,QFP) are :

a) They have closely-spaced leads on all four sides thus allowing for significantly smaller packages relative to the DIP particularly for high pin count chips . From a performance point of view this has also led to a reduction in maximum lead length which is of particular significance in high speed, high pin

count VLSI chips .

b) They are designed for surface mounting on a substrate , rather than for conventional PCB plated-through-hole (PTH) mounting . The significance and implications of the surface mount trend will be elaborated in the next section .

Other new package styles worthy of note indicated in Fig.3 are the following : Tape automated bonding packages (TAB), small outlime packages (SO), flip chip packages and pin grid arrays (PGAs) . Both TAB and flip chip packages will be discussed in the section on multichip modules, where they are expected to play a very significant role . SO packages are observed to be a miniature equivalent of the DIP but with leads bent outward (gull-wing style) to allow for surface mounting, and with closer lead spacing .

Of all the new package styles available, SO packages are the most high pin count limited (Fig.4) . They nevertheless offer important space savings and performance advantages relative to the DIP for medium pin counts and are expected to account for an important segment of the IC package market projected to 1997 (Table 1) . This derives from the anticipated significant growth of surface mounted printed circuit assemblies in the next few years . These are expected to be heavily populated with SO devices, as well as with some of the other increasingly popular surface mount package styles (e.g. PLCC) .

The PGA package deserves special note since it is the only new high pin count VLSI compatible package style intended for conventional PTH printed circuit assembly .

Another device "package" style attracting much attention recently as an effective PCB surface mount option is the bare chip . The concept in itself is not new and has been used for over two decades in hybrid circuit device assembly where high density has been a premium . This assembly approach was called "chip and wire" assembly in hybrid circuits . In SM PCB applications, it has been termed "chip on board" (COB) .

Two major classes of IC packages are worthy of note : plastic packages and ceramic packages . The former are usually intended for general commercial or industrial applications where relatively benign environments are encountered and where the requirements for hermeticity and high reliability are not too strict . Ceramic packages on the other hand are often stipulated for the more demanding military and space environments as well as in harsh industrial environments . Plastic packages are in general significantly cheaper than ceramic packages .

Packages may also be classified into two lead-related categories . All IC packages intended for PTH mounting are evidently leaded . Surface mount packages however come in two variants,

leadless and leaded . Leaded packages are more accomodating of thermal expansion mismatches between the package and the substrate . However they carry the penalty of increased space consumption and the need for careful handling relative to leadless packages . Because of the difficulty of maintaining strict planarity in a plastic package base, surface mount plastic packages are usually leaded .

2.2 The growing trend towards surface mount assemblies

Surface mount assembly is firmly establishing itself as the assembly technology of choice for VLSI , in synergy with VLSI chip packaging trends outlined above .

There are a variety of assembly technologies and techniques for surface mount devices all inherently amenable to a high degree of automation . Although most derive from the same basic assembly principles applied in PTH assemblies (notably solder assembly) , the specific assembly processes in general vary significantly . Wave and hand soldering are commonplace in PTH assemblies while reflow soldering methods are prevalent in surface mount assembly (vapor phase reflow or infrared reflow) [3]. It is also worth noting that component placement /positioning on the substrate is in general a far more critical operation in surface mount assemblies than it is in PTH assemblies , particularly where high density assembly of a large number of close-lead closely spaced packages is involved . In such cases highly sophisticated pick-and-place and automated optical inspection equipment is required . In PTH assembly on the other hand the hole acts as holder/guide for the terminal lead of the device being assembled . Testability is another crucial issue with SM assemblies since the components and leads are closely packed and in addition may be attached on both sides of the substrate further limiting test point accessibility . By contrast, PTH assemblies provide a high degree of test point accessibility at the solder side of the printed circuit .

Furthermore , because of compact packing of devices in SM assemblies, thermal dissipation problems are accentuated . The use of low power dissipation IC device technologies such as CMOS significantly alleviates this problem [4] .

Clearly , an extensive tradeoff comparison between PTH and SM assemblies is beyond the scope of this paper . Whatever the drawbacks of SM assemblies however, their inherent advantages and capabilities clearly outweigh all other considerations particularly when viewed within the context of evolving VLSI/ULSI imperatives for more compact second level interconnection schemes . This fundamental imperative is also coupled with the related imperative associated with level 1 (chip level) interconnection / packaging which has led to the development of the new VLSI package styles

discussed earlier, most of which require SM assembly techniques .

SM assemblies exhibit a higher degree of assembly density/ compaction relative to PTH assemblies for the following major reasons :

a) The inherently smaller size and closer lead spacing of SM packages .

b) The fine line level 2 (printed circuit) interconnection pattern generally required particularly when closely spaced package device leads are involved .

c) The elimination of through -holes for lead mounting which normally consume significant level 2 real estate .

d) The capability for component mounting on both sides of the substrate .

The evaluation above offers a convincing rationale for the current and projected growth trends relating to SM devices and assemblies . These are reflected in Fig.5, where they are compared with trends in PTH assemblies, as well as in multi-chip modules which shall be discussed subsequently . Additional aspects and implications related to SM level 2 interconnection technologies will be further elaborated in the following section where economic consideration will also be addressed .

3 . Trends in Printed Circuit Technologies

3.1 Developments related to conventional printed circuits

Since its introduction over three decades ago the printed circuit has remained the interconnection workhorse of the electronics industry . Printed circuit technology has followed an evolutionary trend that has led to successive significant developments providing increased interconnection capability expressed as increased line density per unit area . The major milestones in this evolution have been the following :

* Single - sided rigid PCBs
* Double - sided rigid PCBs with eyelet connections
* Double - sided rigid PCBs with PTH connections
* Multilayer rigid PCBs with PTH connections
* Multilayer flexible PCBs with PTH connections
* Rigid-flex PCBs with PTH connections

Coupled with these developments has been the incessant

synergistic drive towards achieving finer lines/ finer spaces, vividly expressed in Fig.6 . Fine line technology has progressively improved as a result of cumulative technological developments including :

* Using thinner copper-cladding of the PCB laminate .

* Improving photolithographic materials and processes .

* Using significantly modified printed circuit technologies (e.g. semi-additive and fully additive printed circuit processing [5]).

* Improved control of materials and processes .

A useful quantitative measure of line density per unit substrate area has been proposed , termed connectivity, defined as [6]:

$$C_t = C_o \cdot n$$

where n is the number of layers and C_t is the connectivity per layer (in cm per square cm) . Substrate connectivity is thus clearly enhanced by increasing the number of layers (multilayering) and/or increasing fine line capability .

It is to be noted that printed circuit technology developments were largely prompted by the increasingly imposing interconnection requirements of successive generations of ICs (SSI, MSI, LSI,...) . Two simultaneous objectives were achieved in this regard : higher density interconnections and higher performance interconnections . Performance of an interconnection channel or network is a measure of the transparency it represents to the incoming signal or pulse stream . Any significant signal corruption, attenuation or delay is clearly undesirable . As previously indicated, high speed VLSI devices are imposing increasingly higher performance measures on the interconnection channel or network . A 6-inch PCB path for example may represent a 1 ns path delay . A 10 nanosecond rise time pulse emanating from a medium speed IC gate will not be affected by such a delay . However a high speed IC gate pulse of 1 ns rise time certainly will [7]. Higher density PCB multi-layer technology developments have thus provided an important solution to the mounting requirement for higher speed channels . Finer lines and shorter paths have cumulatively reduced parasitic signal perturbation effects in the interconnection medium .

Substrate electrical characteristics also contribute to interconnection medium propagation speed . In particular, materials with lower dielectric constant help reduce propagation delay and line capacitance . Thus for particularly demanding high speed applications PTFE (teflon) printed circuit substrates with their

lower dielectric constant are preferred over conventional epoxy glass substrates (the added cost penalty notwithstanding) . The trend towards higher speed VLSI based electronic systems is also placing more stringent demands for interconnections with controlled characteristic impedances . This requires maintaining closer control of conductor width and dielectric constant [8] .

It is clear that the choice of an interconnection technology or combination of technologies most cost-effective for a particular application generally involves consideration of many tradeoffs . These may relate to the interconnecting substrate technology per se and often include the essential factors of performance capability , size , cost, and reliability . Other factors related to the assembled substrate also often need to be considered in selecting the most appropriate interconnection technology . Here , such factors as ease of assembly , repairability and testability in addition to assembly reliability and cost, assume prominence .

3.2 Developments in printed circuits for surface mount assembly

Several aspects related to surface mount assemblies and characteristic features of surface mount PCBs have already been addressed in section 2.2 . Additional considerations related to surface mount PCBs are addressed in this section .

From a basic materials and processing point of view , SM PCBs are similar to conventional PCBs . The differences essentially relate to geometric scale : finer lines , shorter paths , smaller (and fewer) through-holes , smaller inner layer via holes , smaller component footprints (associated with active and passive SM components) . These factors combined have led to significantly smaller and more compact surface mount circuit assemblies relative to equivalent PTH circuit assemblies . Typical size reduction ratios are 3:1 . Several of the miniaturization factors indicated above also lead to improved performance (bandwidth characteristics) in the SM PCB interconnection channels, relative to the corresponding PTH PCB interconnection channels . PCB cost considerations also favor SM boards in general . These result essentially from reduced PCB materials and processing costs that derive directly from size reduction . Furthermore because of the higher interconnection density capability , for a particular design, SM boards typically require fewer multilayers than the equivalent PTH board . This consideration also carries important cost implications . Data related to board size , number of layers , and board cost associated with a PTH vs. an equivalent SM circuit implementation is presented in Table 2. The SM approach is clearly more cost effective , even when viewed only at the board level .

However, the total cost impact of implementing an SM approach to equipment physical design is far more profound . System

miniaturization as a result of component and interconnection miniaturization controls the following system elements :

* Number of boards /system
* Frame size
* Backplane complexity
* Connectors and cabling
* Cooling requirements
* Cabinet size

There is in fact a strong correlation between system cost and system miniaturization [4] . (The integrated circuit itself represents a most glaring example of what miniaturization can do to cost !) It has in fact been shown that the relative system cost decreases as the square root of the physical sizes, the volumes , of two alternate packaging approaches [9] .

From a reliability point of view, in a well controlled production environment a properly designed SM assembly should exhibit equivalent or better reliability levels relative to PTH assemblies . Once again the miniaturization concept lies at the root of this consideration .

As with many new and promising technologies however, the conversion route is often far from straightforward . The long and deep-rooted traditions in PTH technologies as well as related investments have often mitigated against a rapid shift to SM technology . New standards and design rules and different / modified specific materials, processes and process controls have meant that a major company seeking to shift to SM technology needs to introduce major changes in its PCB and assembly technologies and practices, in addition to making significant new capital equipment investments as well as investments in training and retraining . The small and flexible company or start-up can probably make a far smoother transition .

The trend towards SM assembly however is powerful and irreversible as expressed in Fig. 5 despite the somewhat slow initial pace in the US and Europe compared to the much more rapid pace of adoption in Japan .

4 . Trends in Hybrid Circuit Technologies

It is evident from previous discussions that SM technology is riding the growth curve primarily because it has offered a satisfactory response to the growing interconnection imperatives of VLSI electronics . In the long term however the technology on its own is not expected to keep pace with future more imposing demands of ULSI (ultra-large scale integration) . New so-called hybrid technologies are presently emerging to serve the related future interconnection

needs . Such technologies however are not entirely new . In fact they are rooted in conventional hybrid technologies which have constituted for almost three decades an important intermediate sector in the interconnection hierarchy (Fig. 1) . Before discussing the new hybrid technology trends a brief review of conventional hybrids is presented which provides an illuminating backdrop to such future developments .

4.1 Conventional hybrid interconnection technologies and circuits

Conventional hybrid circuits essentially consist of two basic parts : a passive substrate, usually ceramic, and assembled miniature active and passive electronic devices . As in printed circuit substrates, the hybrid circuit substrate consists of interconnection patterns that may be multilayered . In addition however it also allows for deposition and in-situ interconnection of planar resistors and, to a lesser extent, capacitors and inductors . Because such substrates consist of deposited film layers of interconnected structures and (passive) components, they are often termed film integrated circuits . These are further classified into thin film integrated circuits and thick film integrated circuits, depending on the materials and process technologies involved .

Thick film circuits are generated by screen printing the required patterns using the relevant paste formulation (conductive, resistive, or dielectric), then imparting the required characteristics by firing in a furnace, after an intermediate drying stage.

Thin film circuits, though apparently structurally similar to thick film circuits , are deposited using vacuum techniques . Patterns are defined using standard photolithography techniques (photoresist imaging and etching) . Thin film processes are thus akin in principle to several processes associated with semiconductor device processing .

Thin film circuits typically offer thinner, finer line patterns relative to thick film circuits . Thick film circuits have a clear advantage in multilayer capability relative to conventional thin film allowing for a generally greater degree of substrate convectivity , C_t , which was defined earlier .

In most applications , thin and thick film integrated circuits are not used as functional circuits in their own right, but as passive substrates onto which are assembled active and passive miniature components, including ICs, resulting in so-called hybrid assemblies, or more specifically thick film or thin film hybrid integrated circuits . These are often completely functional electronic modules that are mounted as "custom components" onto PCB substrates, along with other more standard components such as ICs , transistors, resistors, capacitors, ... Because of their

miniature nature, hybrid assemblies are normally classified as microcircuit components and typically do not exceed 5 sq. inches in area .

It may be clearly inferred from the description above that hybrid integrated circuits fall, in functionality and size , somewhere between a semiconductor integrated circuit and a printed circuit assembly . The hybrid circuit has therefore played a very important historical role as an intermediate interconnection medium that bridges the gap between individual ICs and printed circuit assemblies .

In the U.S. and Europe hybrid circuits have typically been applied in size sensitive military and aerospace applications , with the added benefits of improved performance (speed) and reliability . In Japan, hybrids have largely been used to enhance size and performance capabilities of consumer and industrial products [10] .

Conventional hybrid circuit material and process capabilities and related design rules were eminently suitable for the requirements of intermediate interconnections associated with SSI , MSI and LSI . Thus they offered a satisfactory solution to the relatively limited interconnection bottleneck (or discontinuity) that existed between ICs and printed circuits (both from a size and performance point of view) . However with the growing trend towards higher speed, denser, and more complex VLSI, conventional hybrid circuit capabilities (particularly multilayer fine line) have been coming under increased pressure to meet these rising demands .

Simultaneously , the growth of surface mount technology and related IC device package trends provided an alternate miniaturization path directly via the more conventional and pervasive PCB substrate . These developments are thus partially challenging the traditional role of the hybrid circuit as an intermediate interconnection medium between an IC . It is interesting to note in this regard that there is nothing conceptually new about surface mount technology , which is presently receiving such high acclaim . Indeed , many hybrid circuits are essentially (ceramic substrate) surface mount assemblies . It is small wonder therefore that as PCBs increasingly move to finer line interconnections and surface mount, broadly speaking, the two assembly styles are approaching each other in density , form, function, and performance capability and are thus expected to compete in several market segments . SM PCB substrates typically however allow for much larger single substrate area , while ceramic substrates tend to be relatively restricted in size . On the other hand , the performance edge generally goes to the hybrid circuit .

The comments above notwithstanding , conventional hybrid circuits continue to retain a high degree of cost-effectiveness in

many applications and they are projected to retain a healthy total market growth with thick film far outstripping thin film hybrid integrated circuits [11] . This steady pace has been due to expanding technological capabilities and evolutionary improvements that continue to be made . This is particularly true in thick film circuit developments which have been the most dynamic in the last decade . These have included :

* The development of new thick film materials .

* The development of new substrate materials .

* The development of new and modified processes .

* The development of improved material and process control.

Cumulatively these developments have expanded the cost /performance tradeoffs that the hybrid approach offers . Developments in multilayer fine line capability in particular have provided an intermediate solution to the rapidly growing connectivity demands of state-of-the-art VLSI devices . New and significant initiatives are however currently being actively pursued to provide long term solutions to evolving VLSI requirements . These have involved important departures from current evolutionary technology development trends , and shall be addressed in the following section . Contrary to past hybrid circuit trends, these new initiatives are thin film rather than thick film based .

4.2 Emerging hybrid interconnection technologies for future VLSI/ULSI systems

The most radical developments in interconnection technologies today are those related to so-called high density multilayer interconnects (HDMI) and associated multichip modules (MCMs) . [6,8,12-15] . These technologies relate in principle to the same conceptual multilayer interconnect structures associated with conventional hybrid circuits or multilayer PCBs . The major distinction is in the particular mix of materials and process technologies employed to generate fine line high density structural patterns . These promise an order of magnitude improvement over what is currently feasible with fine line technologies of state-of-the-art multilayer hybrid or printed circuit technologies . The basic elements in these new approaches are the following :

* A trend towards using silicon itself as a substrate material , in addition to utilizing the more conventional ceramic substrate

* The use of multilayer metal/dielectric structures based on polymer materials such as polyimide, and aluminium, copper, or gold conductor materials .

* Utilizing deposition, imaging and pattern generation techniques generally associated with thin film and semiconductor processing (Fig.7) .

* Assembling active devices using the following device types and attach techniques :
  - Bare chip and wire bonding
  - Tape automated bonding (TAB)
  - Flip chip devices

The following clarifications and comments regarding these "new" technologies are in order :

a) The use of a silicon substrate reduces substantially thermal mismatch problems that inherently exist when the substrate material and the chip material are different .

b) The fine line multilayer interconnect pattern generated may approach in future connectivity levels normally associated with silicon wafer multilayer metallization structures since the basic substrate (in the case of silicon) as well as the multilayer metallization processes are to an extent similar .

c) The device package styles indicated above are the most compact of all device package styles available . Flip chip devices provide the smallest footprint on the substrate and are therefore expected to be the most promising for the most density demanding applications .(+)

+ It is interesting to note that the above package styles which hold the most promise for the newly emerging HDMI/MCM assembly technologies are not new at all . In fact chip and wire bonding has been the traditional and prevalent chip attach/connection technique, within chip packages as well as in hybrid assemblies . (Interestingly , such assemblies were often termed multichip hybrids) . Furthermore TAB originated in the early 70s and has since been seeking to make a significant impact in IC packaging and hybrid assembly . As for flip chips, they date back to the early 60s when IBM developed and first used this package style in the IBM 360 mainframe computer family .

d) The use of a silicon substrate provides a potential for developing an "active" substrate onto which external devices such as VLSI components can be assembled using TAB or flip chip techniques [12] . Such high density/high functionality hybrid circuits are currently under development where the active silicon substrate is an IC memory circuit and the assembled chip is a microprocessor [16] .

Before the full potential of these new technologies is realized however, much development work needs to be completed to achieve a better understanding and control of material and process interactions leading to high yield and high reliability . A factor of particular concern in the development and utilization of such high density closely spaced hybrid structures is that of thermal dissipation effects and their reliability impact . A related factor is that of thermal coefficient of expansion (TCE) mismatches , which become particularly significant when integrating and assembling a variety of parts and materials . The thermal dissipation problem is partly alleviated by using low power dissipation VLSI IC device technologies such as CMOS . Clearly however, the development of circuits based on these high density technologies requires that particular attention be paid to thermal design and the related compatibility of materials , processes and structures .

It may be inferred from the previous discussion that HDMI/MCM assemblies are expected to provide a very efficient interconnection medium that would substantially relieve the interconnection bottleneck which has been the focus of this study . In fact these technologies in a sense represent an emerging challenge to the wafer scale integration (WSI) trend presently underway in IC technology whereby fully integrated semiconductor structures and circuits are generated on a full wafer (as opposed to a chip) . The wafer would thus represent a "superchip" several square inches in area . While WSI represents in principle an ideal solution to the interconnection bottleneck many technical hurdles remain . These relate essentially to the difficulty of achieving high chip yield when that chip is an entire wafer . This has led to the need for implementing fault tolerant techniques in WSI designs which in essence compromises full circuit (wafer) utilization and reduces effective connectivity [12] . It is therefore conceivable that HDMI/MCMs may demonstrate more substrate area utilization and connectivity .

5 . The Overall Prognosis

Interconnection trends discussed in this paper have related to the following off-chip technologies :

* Chip packaging technologies
* Conventional printed circuit technologies

* Surface mount printed circuit technologies
* Conventional hybrid circuit technologies
* HDMI/MCM hybrid circuit technologies

Although IC chips per se (as the major interconnection medium for electronic systems) were not addressed in depth, it was emphasized that IC chip density/performance developments have been the major driving force behind the developments related to the technologies indicated above . VLSI developments in particular have prompted new initiatives for the intermediate term and others for the long term (ULSI) .

Intermediate term initiatives have related to surface mount technology and have led to new developments in chip packages, printed circuit boards, and assembly techniques . SM technology in all of these three constituent elements is presently riding the growth curve and is firmly established within current industrial practice . Long term initiatives related to HDMI/MCM hybrid circuit technologies have not yet effectively migrated from the laboratory prototype stage, but major R and D efforts are underway and real growth is expected to begin by the mid 90s . In the meantime evolutionary developments in conventional PCB and hybrid technologies continue apace and are expected to maintain sizeable market share well through this decade, although PTH PCBs are expected to begin showing negative growth by the mid 90s . The projected market trends for conventional (PTH) PCBs, SM PCBs, and MCMs are indicated in Fig.5 .

To an extent, it is expected that printed circuit and hybrid technologies (conventional and new) will compete with each other in various market sectors depending on how the various tradeoffs they present (performance, cost, density, reliability,...) accomodate the particular applications . Overall however, these technologies are expected to complement and reinforce each other . Thus an HDMI/MCM (or a conventional hybrid) may be one (highly complex) component assembled to a PTH or an SM PCB . Similarly, an SM PCB may be assembled to a PTH PCB. Clearly then, all these technologies have an important interconnection role to play in future electronic systems . An entirely different interconnection technology that is still in the basic exploratory stage is that of optical interconnections in the form of integrated waveguides or "optical wires" [7,12] . Despite its promises , its ultimate impact as a cost-effective interconnection medium is presently a matter of speculation .

To further highlight the significance of the developments and trends discussed in this study , reference will be made in what follows to several illuminating charts and figures .

a) Table 2 displays trends in interconnection limits for plug-in circuit packs in telecommunication systems [1] . The progressive increase in complexities and interconnection requirements has necessitated the move to both finer line printed circuits and

greater PCB multilayer capability .

b) Fig.8 presents data relating to interconnection cost vs. density of the following interconnection media : double-sided rigid PCBs, multilayer PCBs and high density hybrid integrated circuits, and CMOS IC chips [1] . The figure clearly demonstrates the one to two order of magnitude improvement in interconnection density as well as in cost in moving interconnections on-chip rather than providing them off-chip .

c) Table 3 presents a range of very indicative comparative data relating to the various interconnect technologies discussed [6] . The table provides added evidence of the overwhelmingly efficient interconnection capability of silicon ICs .

d) Fig.9 provides another useful perspective on the relative connectivity of the various interconnection technologies measured against substrate efficiency, FA, defined as [6] :

$$F_A = \frac{\text{active silicon cell area}}{\text{total substrate area}}$$

Fig.9 vividly displays the long march of interconnection technologies towards bridging the interconnection gap with silicon ICs .

e) Fig.10 illustrates the cost per unit area of the different interconnection technologies as a function of interconnection density [6] . The PCB density-cost curve is seen to eventually lead to prohibitive substrate costs as the number of layers approaches 20 . HDMI/MCMs are observed to provide more cost effective solutions for such interconnection density requirements .

f) Fig.11 summarizes the inexorable trend in electronic systems evolution towards the achievement of higher performance and lower cost , in less physical space [7] : The increasing scale of integration and the concomitant reduction in feature size characteristic of "microintegration" have been major factors underlying these system trends . Macrointegration in the future is expected to play an increasingly significant analogous and complementary role .

In addition to the system benefits reflected in Fig.11, the final table , Table 4, very vividly illuminates the system reliability impact of an increasing scale of integration . the hypothetical system in question consists of 100,000 gates and comparative figures are given in Table 4 for successive system realizations based on the utilization of devices with 100, 1000, and 10,000 gates respectively [1] . The analysis assumes a FIT count of 50 for all the ICs . (FIT stands for failures in 10^9 hours) . This assumption is reasonably valid since it has been found that IC FIT count, for a given IC technology and manufacturer, is roughly constant, independent of the number of gates per chip .

In the example FIT counts for PCB assemblies, appropriate to the board types required at the various levels of integration have been used . The specific system FIT counts in this idealized simplified example are not important in themselves . What is important to note however is the clear trend towards significantly higher system reliability levels as a result of increased levels of integration .

6 . Implications for Future Oriented Arab Electronics Industries

The elements and factors that need to be mastered, provided, or controlled before Arab electronics industries can secure a place under the sun are many and varied . Several will no doubt be deliberated in this First Arab Electronics Conference/Exhibition . They range from device , circuit and system development and design, to supply, manufacturing, investment and financing , marketing and distribution, in addition to other more salient but highly significant factors relating to the overall operational environment within which electronics activities can prosper .

The emphasis placed in this study on interconnection technologies has been intended to highlight the need for the initiation and sustenance of purpose-oriented R and D programs in these domains at Arab institutions concerned with the development and manufacture of electronic products .

In an increasingly competitive electronics global world environment, the success of Arab electronics industries in the future will hinge on the development and manufacture of electronics products that embody on the functional level the most cost-effective innovations in device , circuit , and system electronic design , and on the physical level the most cost-effective innovations in device, circuit , and system interconnection and packaging design . Furthermore, cost-effective product development in the future will increasingly require that product electronic design and physical design be undertaken simultaneously and interactively during the product development cycle .

APPENDIX

Activities in Interconnection Technologies at the Scientific Studies & Research Center in Damascus, Syria

The significance of electronic interconnection technologies has been recognized at SSRC for several years . Development activities in several technologies have been progressively set up in the following areas :

1 - Printed circuit technologies :

Single-sided and double-sided through-hole PCB technologies have been in place for some time . Multilayer, flexible , semi-additive and surface mount PCB technologies and related assembly techniques are currently being investigated .

2 - Hybrid integrated circuit technologies :

Basic thick film hybrid integrated circuit capability is presently available . Efforts to provide improved multilayer and fine line capability and related assembly techniques are currently underway .

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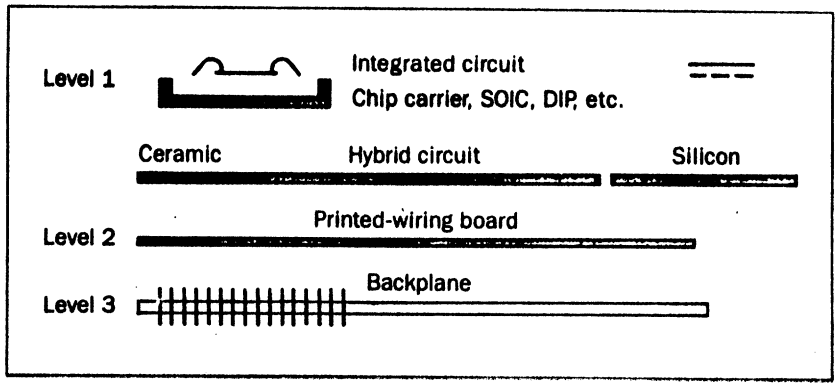
Figure 1: Interconnection levels. DIP = dual in-line package; SOIC = small outline integrated circuit.



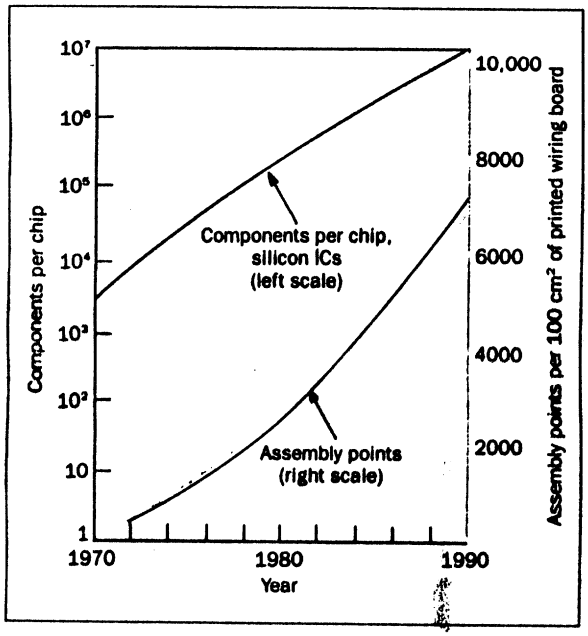


Figure 2: The history of silicon integrated circuit scale of integration and its effect on interconnection density.

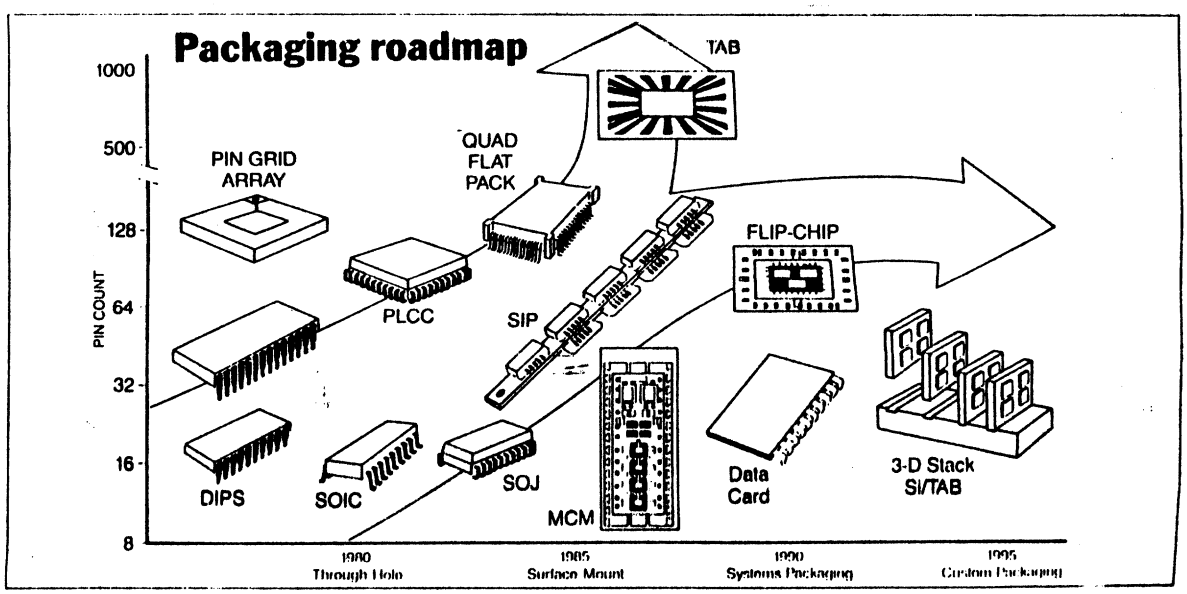


Figure 3: Device package styles

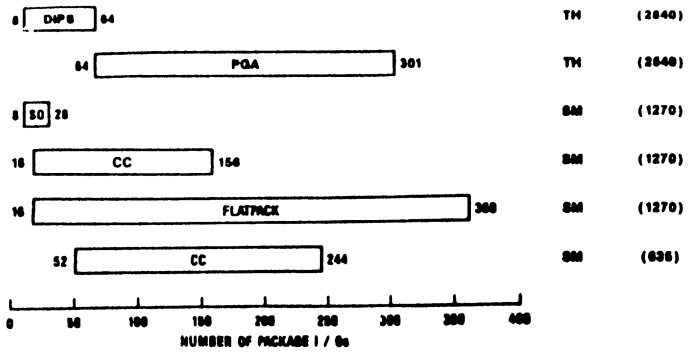
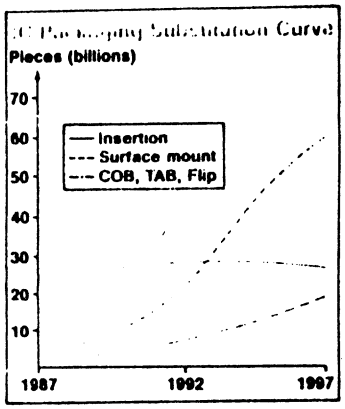


FIGURE 4
IC package types as a function of I/Os and method of attachment to PWBs.

Table1: Quantity (billion) 1997

DIPs	16.6
SIPs/ZIPs	2.8
PGAs	1.5
Socketed SM	7.0
Flat packs & others	0.6
Hermetic CCs	0.9
SOs	32.0
Plastic: PLCCs	6.6
PQFPs	16.0
TAB	7.9
COB	7.1
Flip chip	7.0
Total	105.0



BPA forecasts that MCMs will emerge as a major IC packaging technology in 1997.
Figure 5

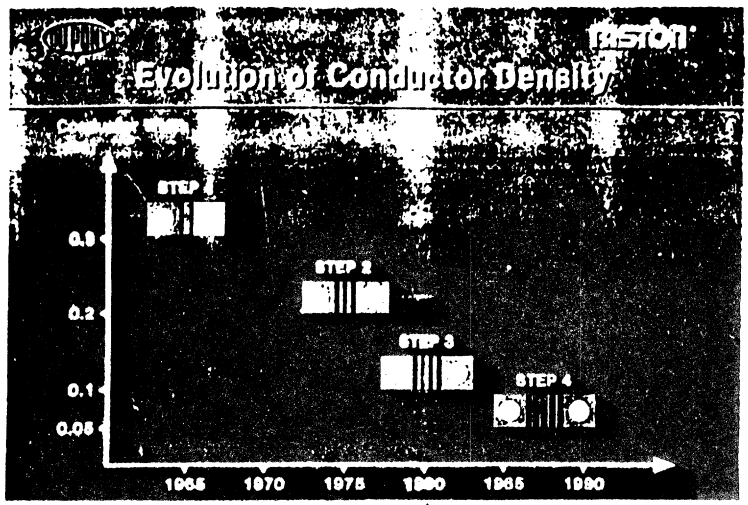
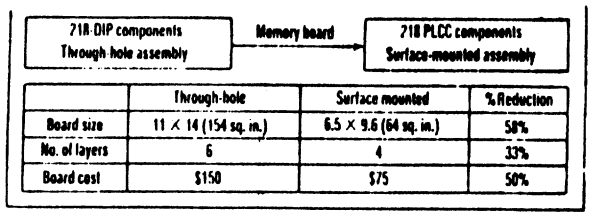


Figure 6

Table 2: Relative cost of PTH vs SM PCB s



	Through-hole	Surface mounted	% Reduction
Board size	11 × 14 (154 sq. in.)	6.5 × 9.6 (64 sq. in.)	58%
No. of layers	6	4	33%
Board cost	$150	$75	50%

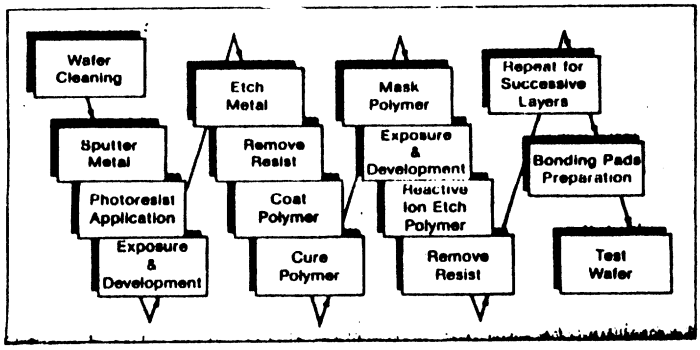


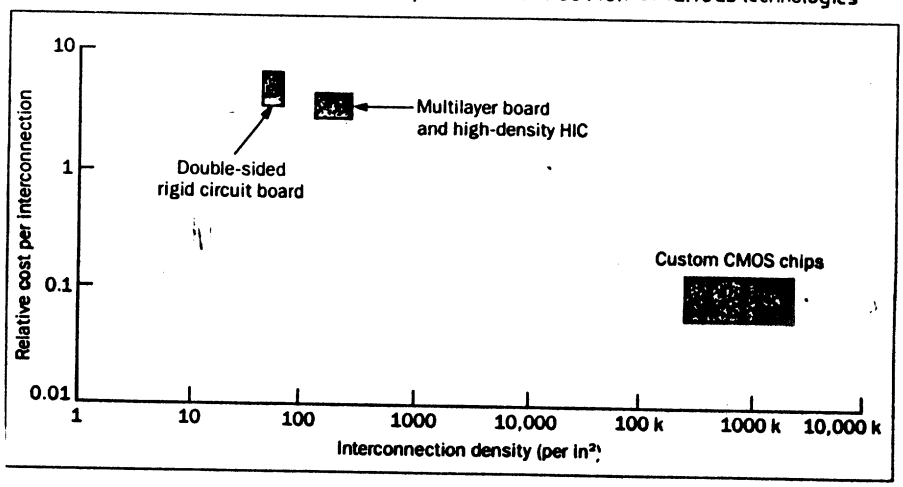
Table 3: Interconnection Limits for Telecommunication Systems

Pacing technologies	Typical limits for plug-in circuit packs 1970	1978	1986	Early 1
Circuit pack size, in²	50	100	200	
Layers of printed wiring	2	6	8	
Line widths, mils	25	7	6	
Connections (number of connected device terminals)	100	2000	9000	
External input/outputs	80	300	600	
Logic gates	10^3	10^4	10^5	

TABLE 4
CONNECTIVITY VALUES FOR INTERCONNECT TECHNOLOGIES

Conductor Line Width, microns	Conductor Pitch, microns	Connectivity per level, cm/cm²	Interconnect Technology
250	500	20	pcb, thick film hybrid
125	250	40	thick film hybrid, state-of-the-art, cofired ceramic
100	200	50	pcb, state-of-the-art
62.5	135	75	microwire
25	100	100	medium film on polyimide
10	40	250	medium film on polyimide, state-of-the-art
2	6	1570	LSI SIC
1	3	3100	VLSI SIC

Figure 8: Relative cost per interconnection for various technologies



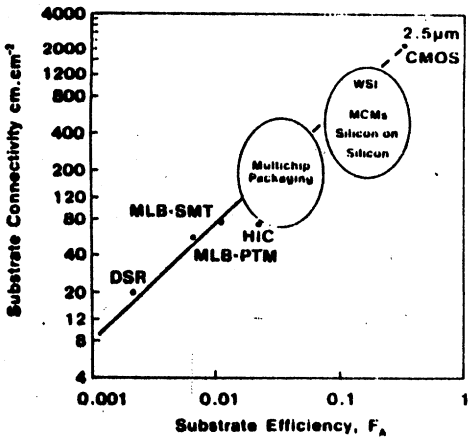


Fig. 9: Connectivity versus substrate efficiency for different technologies.

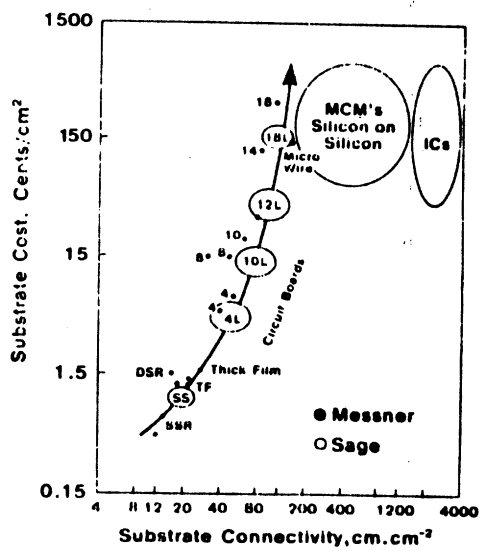


Fig. 10: Substrate cost versus connectivity.

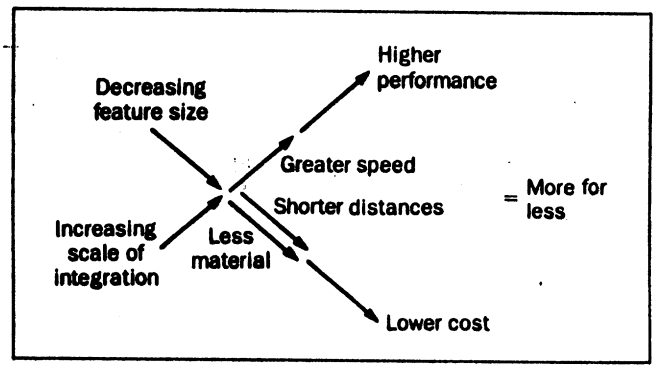


Figure 11: Trends in electronic packaging.

Table 5: Effect of Increasing Scale of Integration on System Reliability

	Gates per IC		
	100	1000	10,000
Number of ICs	1,000	100	10
IC FIT count, total	50,000	5,000	500
Numer of external interconnections	40,000	12,600	4,000
Interconnection FIT count, total	4,000	750	200
System FIT count	54,000	5,750	700